

IN THE CLAIMS:

Pease cancel claims 28-33 without prejudice.

1. (Previously Presented) A method for repairing a memory device having at least one array of memory cells arranged in rows and columns with each row further divided into a plurality of words, the method comprising:

detecting defective storage cells;

replacing at least one of a row or column containing one or more defective storage cells with a redundant row or column; and thereafter

replacing at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word.

2. (Original) The method of claim 1, further comprising allocating redundant rows or columns used for replacement among rows or columns, respectively, based on the number of defective storage cells contained therein.

3. (Original) The method of claim 2, comprising allocating a redundant row or column to a first row or column containing defective storage cells in preference over a second row or column containing a lesser number of defective storage cells.

4. (Original) The method of claim 3, further comprising replacing the defective storage cells of the second row or column with one or more redundant words.

5. (Original) The method of claim 4, wherein one redundant word replaces defective storage cells of at least two columns.

6. (Original) The method of claim 4, further comprising activating a FAIL signal to indicate the memory device is not repairable if all defective cells detected cannot be replaced.

7. (Original) The method of claim 1, wherein the method is performed as part of a built-in self test (BIST) of the memory device.

8. (Original) The method of claim 7, wherein the BIST serves multiple memory devices with embedded and shared redundant elements.
9. (Original) The method of claim 1, wherein detecting defective storage cells comprises conducting a column test.
10. (Original) The method of claim 9, wherein conducting the column test comprises identifying and storing addresses of columns having greater than a threshold number of defective storage cells.
11. (Original) The method of claim 10, wherein the column test comprises overwriting addresses of columns having a first number of defective storage cells with addresses of columns having a second number of defective storage cells, wherein the second number is greater than first number.
12. (Original) The method of claim 9, wherein detecting defective storage cells comprises conducting a row test.
13. (Original) The method of claim 1, wherein detecting defective storage cells comprises conducting a row test.
14. (Original) The method of claim 13, wherein conducting the row test comprises identifying and storing addresses of rows having greater than a threshold number of defective storage cells.
15. (Original) The method of claim 14, comprising replacing defective storage cells of rows having greater than the threshold number of defective storage cells with redundant words.
16. (Previously Presented) A self-repairing memory device comprising:
 - at least one array of storage cells arranged in columns and rows, with each row comprising multiple words;
 - at least one of redundant row or column elements for replacing rows or columns containing defective storage cells;

at least one block of redundant word elements for replacing words containing defective storage cells without replacing the entire rows containing the words being replaced; and

built-in self repair (BISR) circuitry configured to replace at least one of a row or column containing one or more defective storage cells with a redundant row or column and, after completion of the replacement of the at least one of a row or column by the redundant row or column, to replace at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word.

17. (Cancelled)

18. (Original) The self-repairing memory device of claim 17, wherein:

the built-in self repair (BISR) circuitry is configured to allocate redundant row or column elements to rows or columns containing defective storage cells based on the number of defective storage cells contained therein.

19. (Original) The self-repairing memory device of claim 18, wherein:

the built-in self repair (BISR) circuitry is configured to replace, with redundant word elements, defective storage cells contained in rows or columns not allocated redundant row or column elements.

20. (Original) The self-repairing memory device of claim 18, wherein:

the at least one array of storage cells comprises multiple arrays of storage cells;
and

at least two of the arrays of storage cells share the block of redundant word elements.

21. (Original) The self-repairing memory device of claim 18, wherein:

the at least one array of storage cells comprises multiple arrays of storage cells;
the at least one of redundant row or column elements for replacing rows or columns containing defective storage cells comprises redundant row elements and redundant column elements; and

each array of storage cells is provided with at least one BISR circuit.

22. (Original) The self-repairing memory device of claim 16, wherein the storage cells are dynamic storage cells.

23. (Original) The self-repairing memory device of claim 16, wherein the built-in self repair (BISR) circuitry comprises:

row test circuitry; and

a plurality of registers to store address of rows containing at least a first threshold number of defective memory cells, as detected by the row test circuitry.

24. (Original) The self-repairing memory device of claim 23, wherein the built-in self repair (BISR) circuitry further comprises:

column test circuitry; and

a plurality of registers to store address of columns containing at least a second threshold number of defective memory cells, as detected by the row test circuitry.

25. (Original) The self-repairing memory device of claim 16, wherein the built-in self repair (BISR) circuitry comprises:

column test circuitry; and

a plurality of registers to store address of columns containing at least a threshold number of defective memory cells, as detected by the column test circuitry.

26. (Original) The self-repairing memory device of claim 16, further comprising:

a bank of non-volatile storage elements to store addresses of at least one of rows or columns to be replaced with redundant rows or columns.

27. (Original) The self-repairing memory device of claim 16, further comprising a memory built-in self test (BIST) circuit to identify defective storage cells.

28-33. (Cancelled)

34. (Previously Presented) A memory built-in self repair device, comprising:

a plurality of memories, each of said memories having an array of storage cells arranged in columns and rows, with each row comprising multiple words,

a plurality of memory built-in self repair circuits, each memory built-in self repair circuit being associated to one of the plurality of memories, and

at least one block of redundant word elements for replacing words containing defective storage cells without replacing the entire rows containing the words being replaced, wherein one block of redundant word elements is used for replacing words containing defective storage cells of the plurality of memories, and wherein replacing of the at least one word with a redundant word is accomplished after replacement of all rows or columns with redundant rows or columns.

35. (Cancelled)